Appendix "UA"
Ideal Power UL 1741 SA Advanced Inverter Features

Applicable Ideal Power Converter Models:
- Stabiliti 30C/30C3
- SunDial 30PV/30PVF/30PV+S/30PVF+S

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1.0 How to Use This Document

This document describes the basic functions of the advanced features as described in UL1741 SA and California's Rule 21. Specifics on the registers via Modbus and their ranges will be described. The intent of this document is to provide the operator with the bases of programming these features within the certified range to support the SRD from the local utility.

This document does not describe the basic functionality of the PCS nor does it describe any of the registers or converter features that are not related to UL1741 SA or California's Rule 21. Please refer to other Ideal Power documents such as the appropriate Installation and Operations Manual, Quickstart Guide and register maps for such information.

2.0 Introduction to UL1741 SA & Rule 21

What is UL1741 SA, and why is this standard important?

- Today, utility interconnection requirements (IEEE 1547) require Distributed Generation (DG) devices, such as traditional PV Inverters, and Ideal Power's bidirectional dual and multiport Converters to disconnect, and immediately shut down all power flows, when the grid is experiencing stability issues.
- The UL1741 SA specifies both new smart inverter features and their related test methods. Once certified to the UL1741 SA standard and approved for grid interconnection, these advanced DG devices will stay online and adapt their output and behavior to further stabilize the grid during abnormal operation rather than simply disconnecting.
- Bottom Line? Modernizing the world's electric grids is a critical enabler for achieving broader societal benefits and avoiding brownouts or blackouts that come from optimizing the way we generate, distribute and use electricity. Once deployed, advanced DG devices with UL1741 SA functionality as described in this document, should increase the reliability and stability of the grid.

What is Rule 21, and why is it important?

- The Rule 21 tariff is the inverter related content to the State of California Electric Tariff Rule 21 developed by the California Public Utility Commission (CPUC).
- Rule 21 is a Source Requirement Document (SRD) that is used with UL1741 SA. SRDs define the specific DG device configuration parameters to be used with UL1741 SA.
- The state of California has announced that inverters installed in the state will be required to comply with the Rule 21 tariff within one year of the publication of the UL1741 SA. That date is on or about 9/8/17.
- Areas containing high levels of DG and solar penetration, such as Hawaii have also created their own specific SRD's, designed to serve the unique needs of their local grid.
- Outside of California and Hawaii, other SRDs will be defined as grid operators look to add advanced DG devices to further modernize their local area electrical power system.

What is Phase 1?

- Phase 1 is the first step in a multi-step/multi-year process to define, certify and introduce UL1741 SA compliant DG devices into the grid.
- Phase 1 DG devices operate autonomously, without remote intervention or control.
- As noted, Phase 1 autonomous features include: the ability to "ride-through" wider ranges of voltage and frequency fluctuation; the capability to actively counteract point

of interconnection voltage changes; and, a "soft-reconnect" capability to avoid sharp power spikes when large numbers of DG devices reconnect to a distribution system.

- Phase 2 and 3 will require additional advanced features, including remote control and communication of DG devices. *These features and capabilities are not yet available, nor completely defined, and are beyond the scope of this document.*

3.0 Overview of UL 1741 SA Advanced Inverter Features

3.1 Autonomous Volt-Var Operation

Volt-Var control allows the Converter to counteract voltage deviations from nominal grid voltage as measured at the Point of Common Coupling (PCC) by consuming or producing reactive power, in response to over or under-voltage events. The Converter's Volt/Var response helps to maintain voltage stability: better supporting "weak" circuits that may be encountered on long distribution feeders with high levels of PV penetration, or other distributed generation resources.

The amount of reactive power available can be established by a "curve" defining voltage versus percentage of reactive power. The percentage of reactive power can be calculated as:

- **Percentage of available reactive power** for the measured percentage of the reference voltage. "Available Vars" implies the consumption or production of reactive power that does not affect the real power output.
- **Percentage of maximum reactive power**. In this case, consumption or production of reactive power may impact the real power output.

The Volt/Var curve is shown in the figure below. There are 4 voltage setpoints: V1, V2, V3 and V4. V2 and V3 make up a dead-band, within that dead-band voltage range, the converter will not produce or consume reactive power, in response to an over or under voltage condition as measured at the PCC. There are 2 Q (reactive power) setpoints: Q1 and Q4, that relate to V1 and V4. The Converter's AC1 port must be configured as either the FPWR, GPWR, or NET Control Method in order to enable Volt-Var operation.

- *The Converter's factory default for autonomous Volt-Var control is OFF (disabled).*

Figure 1: Volt/Var Setpoint Example

Benefits of Volt-Var

Permitting active voltage regulation will allow permit interconnected distributed energy resources, such as PV Inverters and Ideal's bidirectional Converters to compensate for any voltage impacts that their generation might have on the circuit, and can also help maintain conservation voltage reduction (CVR) voltage levels and stabilize voltage deviations caused by other distributed resources and loads.

3.2 Autonomous Frequency-Watt Operation

Frequency-watt control is used to limit the Converter's active power generation or consumption when the grid deviates from its 60 Hz nominal frequency by a specified amount.

Similar the Volt/Var example above, the Converter's response will help stabilize grid frequency.

Frequency-Watt utilizes a set frequency-watt pairs: a set of frequencies and their corresponding Watt setpoints that will be treated as a piecewise linear function. The frequency setpoint is the actual frequency in Hertz. The watt setpoint is 0% to 100% of the maximum available watts. In an energy storage system, the watt setpoint may be negative to indicate the system should absorb power from the grid to lower the frequency even further. Point F3 (start derate at this frequency); F4/P4 (max frequency / max derate) define the slope and shape of the Frequency-Watt curve.

The Converter's AC1 port must be configured as either the FPWR, GPWR, or NET Control Method in order to enable Frequency-Watt operation.
- *The Converter's factory default for autonomous Frequency-Watt control is OFF (disabled).*

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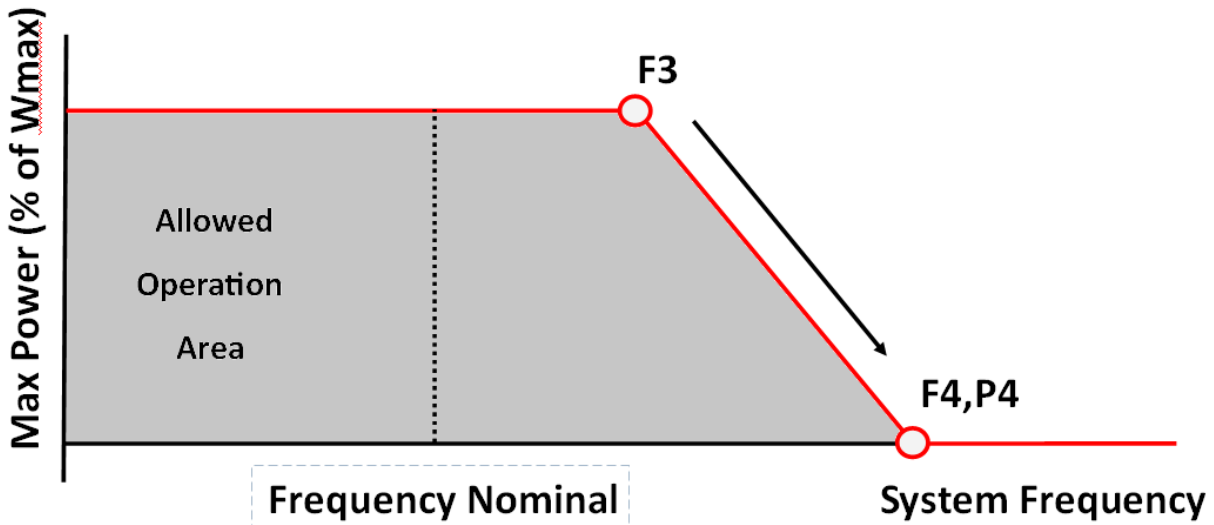
Figure 2: Frequency-Watt Setpoints

Benefits of Frequency-Watt

Permitting active frequency regulation will allow permit interconnected distributed energy resources, such as PV Inverters and Ideal's bidirectional Converters to compensate for any frequency impacts that their generation might have on a circuit, and can also help maintain and stabilize frequency deviations caused by other distributed resources and loads.

3.3 Autonomous Volt-Watt Operation

Volt-Watt control allows the Converter to control output power based on the voltage measured at the point of common coupling (PCC). A set of 2 (V3 and V4) voltage setpoints and their corresponding watt P4 setpoint are treated as a piecewise linear function. The voltage is defined as a percent of VRef, the voltage at the point of common coupling. The watt setting is 0% to 100% of the maximum available watts (WMax). The Converter's AC1 port must be configured as either the FPWR, GPWR, or NET Control Method in order to enable Volt-Watt operation.

- *The Converter's factory default for autonomous Volt-Watt control is OFF (disabled).*
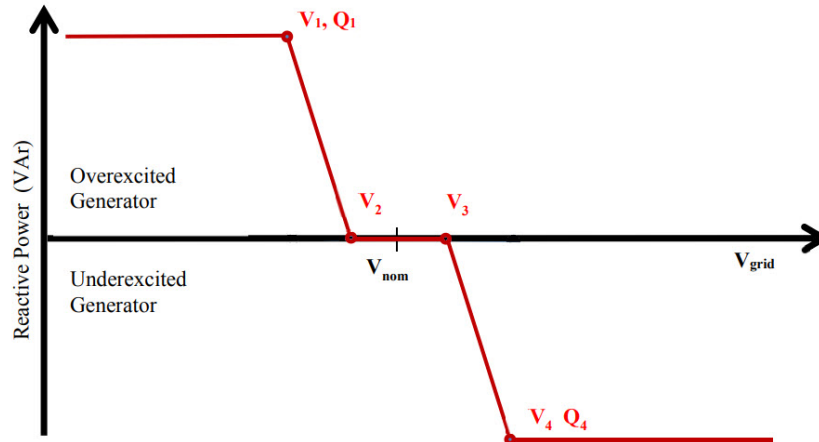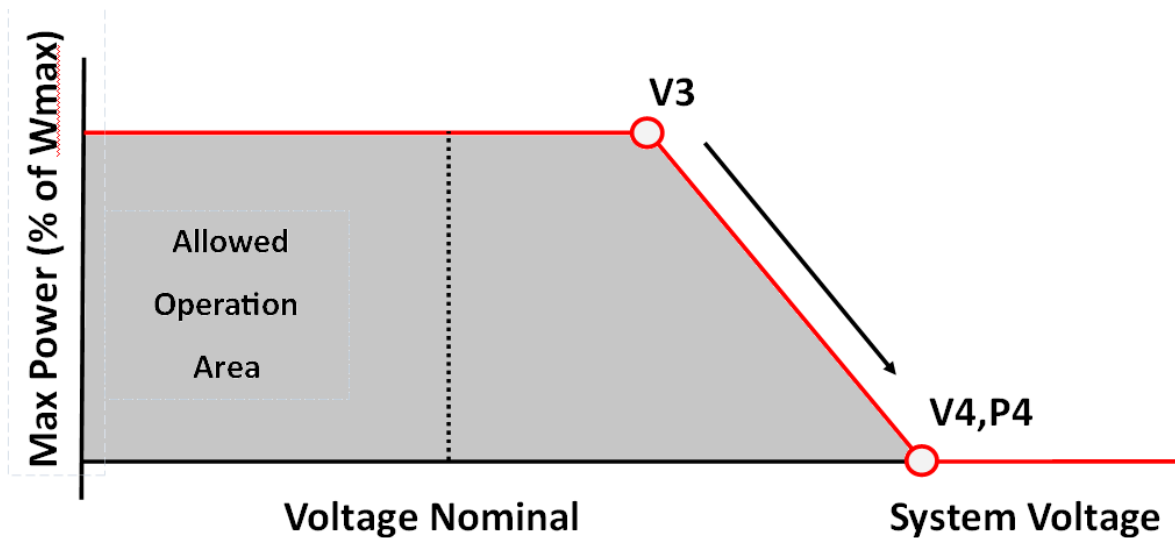
Figure 3: Volt-Watt Setpoint Example

Benefits of Volt-Watt

Enabling active voltage regulation allows interconnected distributed energy resources, such as PV Inverters and Ideal's bidirectional Converters to compensate for any voltage impacts that their generation might have on a circuit, and can also help maintain and stabilize voltage deviations caused by other distributed resources and loads.

3.4 LVRT Operation

Text and diagrams formally found in Section 3.4 has been merged into Section 3.5 to simplify content management.

3.5 HVRT Operation (includes Section 3.4)

For low and high voltage line conditions, the Converter responds to a set of of volt-duration pairs: voltage levels and duration (time) are treated as a piecewise linear function. There are different voltage and duration setpoints representing a "Must Disconnect" region, and another set for a "Must Remain Connected" region. Both the Must Remain Connected and Must Disconnect curves support up to six unique volt-duration pairs. Voltage setpoints are defined as percent of VRef, the voltage sensed at the point of common coupling.

Note that the Converter will disconnect and generate a low-voltage (or high-voltage) fault if any of the Must Disconnect volt-duration pairs are satisfied.

- *The Converter's factory default for LVRT/ HVRT is ON (enabled).*

Note that UL1741 SA requires that the Converter to support an additional level of complexity to the LVRT/HVRT features described above. An additional group of duration "cessation zone" setpoints are defined, which dictate a new Converter behavior in the presence of a "near" LVRT/HVRT fault.

The Converter will cease real power export, but DOES NOT disconnect, nor fault during the defined cessation period. If the cessation period is not exceeded, the Converter will immediately return to service at its programmed real power level (kW), utilizing a predetermined ramp rate setpoint.

If the cessation period is exceeded, the Converter DOES disconnect and generates a LVRT/HVRT fault, which starts its internal reconnect timer.

- *The Converter's factory default for LVRT/HVRT cessation is ON (enabled).*
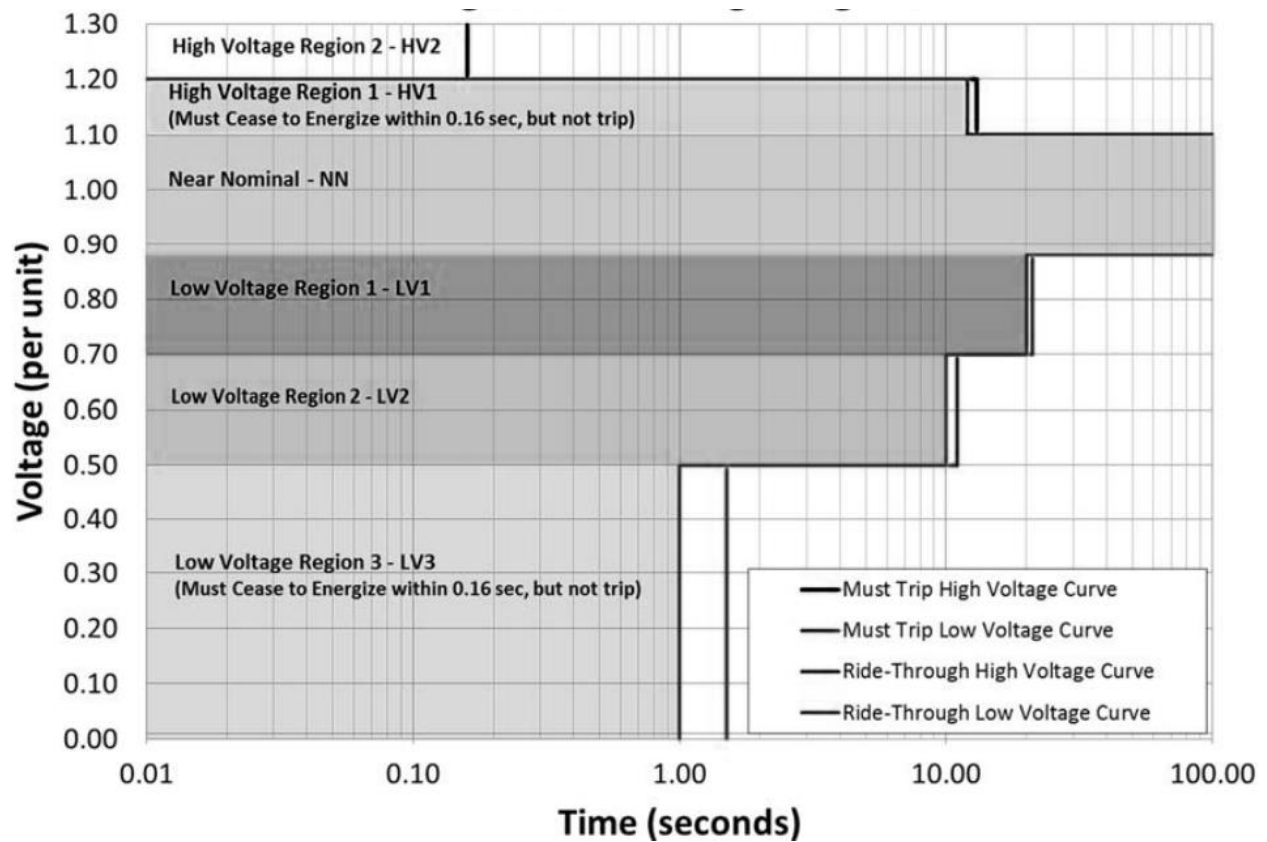
Figure 5: HVRT/LVRT Example

Benefits of LVRT/HVRT

The expansion of low and high voltage protection limits permits interconnected distributed energy resources, such as PV Inverters and Ideal's bidirectional Converters to ride through temporary voltage sags and peaks, decreasing the number of unnecessary disconnections by such systems, which can result in prolonged power outages.

Benefits of LVRT/HVRT Cessation

With cessation enabled, the Converters will temporary cease to export, during very brief LVRT or HVRT events. However, unlike a disconnect event, which generates a fault condition, and subsequent reconnect timer countdown, the converters will resume export immediately, to better support the grid after brief LVRT or HVRT events clear.

3.6 LFRT Operation

Text and diagrams formally found in Section 3.6 has been merged into Section 3.7 to simplify content management.

3.7 HFRT Operation (includes Section 3.6)

The LFRT/HFRT model is a set of duration-frequency pairs for low and high frequency line conditions that will be treated as a piecewise linear function similar to that shown above for LVRT/HVRT. A single LFRT/HFRT model is provided with a "Must Disconnect" curve. Unlike LVRT/HVRT, no corresponding "Must Remain Connected" curve is provided.

- *The Converter's factory default for LFRT/HFRT is ON (enabled).*

As with LVRT, UL1741 SA also requires the support a LFRT/HFRT cessation feature.

- *The Converter's factory default for LFRT/HFRT cessation is ON (enabled).*
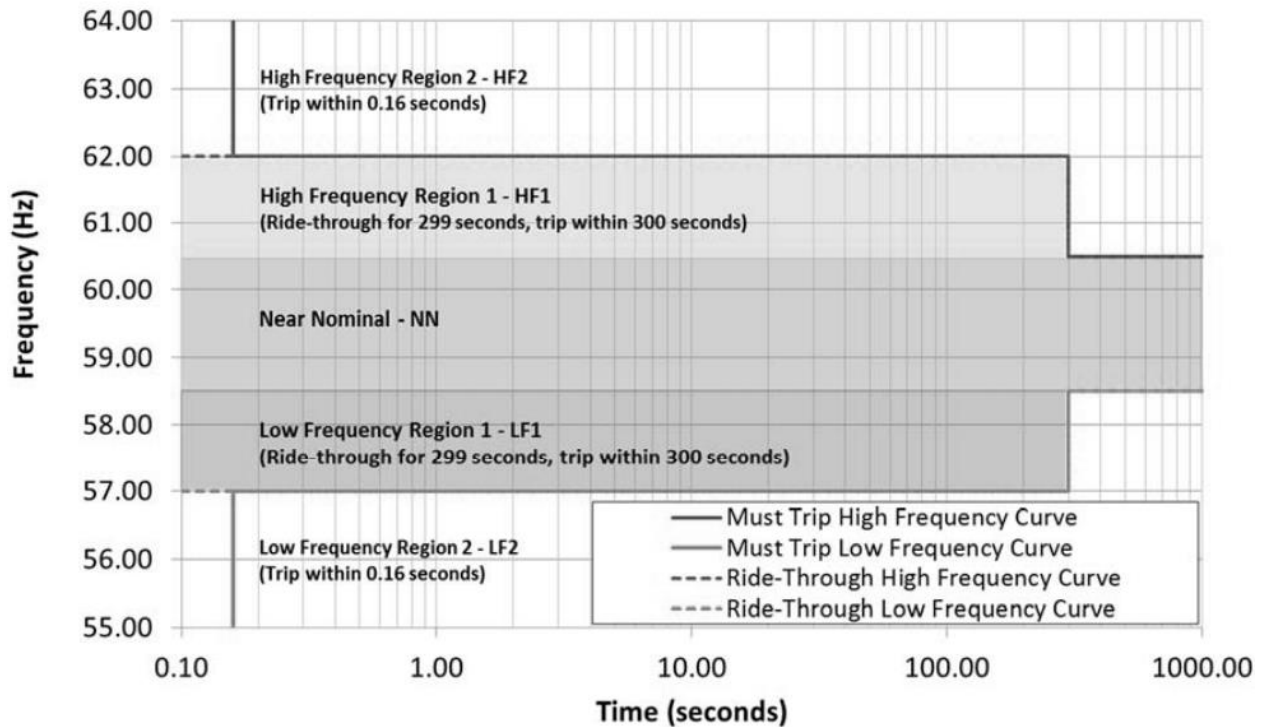
Figure 6: HFRT/LFRT Example

Benefits of LFRT/HFRT

The proposed expansion of low and high frequency protection limits will permit interconnected distributed energy resources, such as PV Inverters and Ideal's bidirectional Converters to ride through temporary changes in frequency, thus decreasing the number of unnecessary disconnections by such systems, which can result in prolonged power outages.

Benefits of LFRT/HFRT Cessation

With cessation enabled, the Converters will temporary cease to export, to support the grid during very brief LFRT or HFRT events. However, unlike a disconnect event, which generates a fault condition, and subsequent reconnect timer countdown, the converters will resume export immediately, after brief LFRT/HFRT events clear, to better support the grid.

3.8 Normal Ramp Rate

UL1741 SA has a defined normal ramp rate setpoint for real power (kW) for use with both PV Inverters, as well as Ideal's bidirectional Converters. The normal ramp rate, expressed in Watts/second establishes both ramp-up and ramp-down rates, to smooth the transition from one output power level to another output power level.

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- *The default factory normal ramp rate is 1kW per second, and it is ON (enabled).*

Benefits of Normal Ramp Rate

Establishing the use of soft ramp rates at reconnect will help avoid sharp transitions and the consequential power quality problems of voltage spikes or dips, harmonics, and oscillations, as disconnected Converters return to an online and power export state.

3.9 SPF - Specified Power Factor Operation

The Converter supports a specified power factor (PF) control feature: the programmable PF range is from .75 leading to .75 lagging; with maximum Converter Apparent Power of 32 kVa. Using a leading (positive) and lagging (negative) sign convention, the Converter is capable of operation in all four quadrants. *All IPWR PCS' use the IEEE power factor sign convention (positive in quadrants 2, 4; negative in quadrants 1, 3).*

The Converter's AC1 port must be configured as the NET Control Method in order to enable Specified Power Factor operation

- *The Converter's factory default for autonomous Specific Power Factor control is ON (enabled), with a PF setpoint of 1 (unity).*
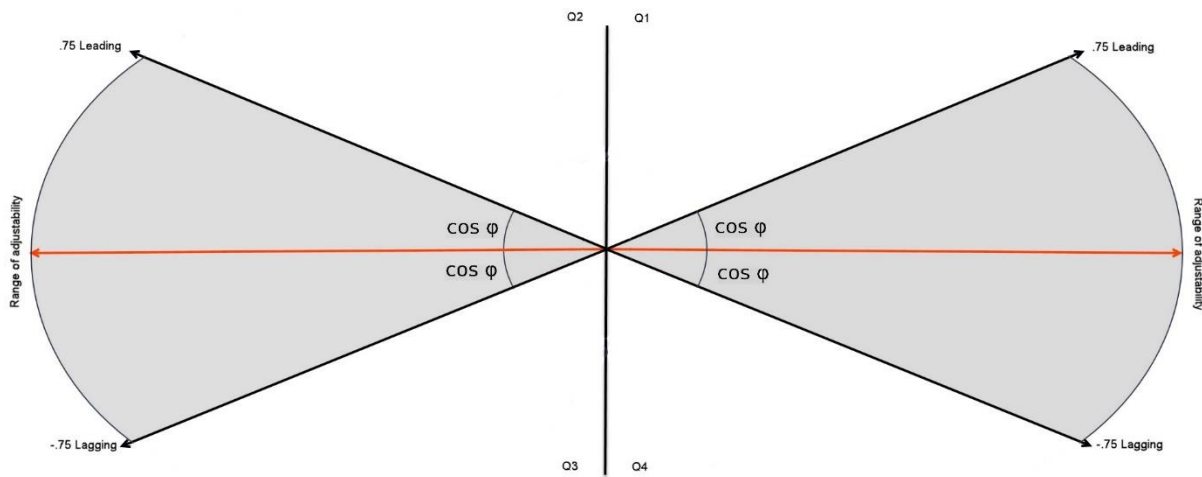
Figure 4: Specified Power Factor Example

Benefits of Specified Power Factor

Establishing adjustable power factors can help offset the power quality issues caused by different types of loads and the possible impacts of different types of distributed energy

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resources, such as PV Inverters and Ideal's bidirectional Converters. This will permit the circuits to better maintain the optimal power factor of 1.0.

3.10 Soft-Start Ramp Rate

In the event of a fault condition, such as Converter trip due to LVRT/HVRT conditions, or LFRT/HFRT conditions being met, the Converter will re-establish its connection to the grid after the fault clears.   The Converter will ramp its power up after the connection is established and it's reconnect countdown is complete.

- *The default factory soft-start ramp rate is 1kW per second, and it is ON (enabled).*

<u>Benefits of Soft Ramp Rate</u>
Establishing the use of soft ramp rates at reconnect will help avoid sharp transitions and the consequential power quality problems of voltage spikes or dips, harmonics, and oscillations, as disconnected Converters return to an online and power export state.

4.0 Source Requirements Document (SRD)

In early-to mid 2017, the three major investor-owned utilities (IOUs) in California: SDG&E, PG&E, and Southern California Edison established a common SRD for Phase 1 deployment of UL1741 SA compliant DG devices. Although subject to change by jurisdiction, or area specific interconnection agreement, all Ideal Power Converters utilize this common SRD for their factory default settings.   The four tables below, and corresponding text reflect those factory settings, and were sourced from SDG&E's most recent Rule 21 tariff, which was published on 3/30/17.

I. Default Activation States for Phase 1 Functions

Unless otherwise provided by Distribution Provider, pursuant to Distribution Provider's Distribution Generation Interconnection Handbook, the default settings will be as follows:

i) Anti-islanding – activated

ii) Low/High Voltage Ride-Through – activated

iii) Low/High Frequency Ride-Through – activated

iv) Dynamic Volt/Var operations – deactivated

v) Ramp rates – activated

vi) Fixed power factor – activated

vii) Reconnect by "soft-start" methods – activated

These default activation states may be modified by mutual agreement between Distribution Provider and Producer.

Table 1: Ideal Power Factory Default Activation States (source SDG&E).

Power Factor

Producer shall provide adequate reactive power compensation on site to maintain the Smart Inverter power factor near unity at rated output or a Distribution Provider specified power factor in accordance with the following requirements:

i) Default Power Factor setting: 1.0 +/- 0.01 (0.99 Lagging to 0.99 Leading)

ii) Aggregate generating facility is greater than 15 kWw: : 1.0 +/- 0.15 (0.85 Lagging to 0.85 Leading) down to 20% rated power based on available reactive power

iii) Aggregate generating facility is less than or equal to 15 kW: : 1.0 +/- 0.10 (0.90 Lagging to 0.90 Leading) down to 20% rated power based on available reactive power

Table 2: Ideal Power Factory Default Power Factor Setpoints (source SDG&E).

Ramp Rate Requirements

The Smart Inverter is required to have the following ramp controls for at least the following four conditions. These functions can be established by multiple control functions or by one general ramp rate control function. Ramp rates are contingent upon sufficient energy available from the Smart Inverter.

i) **Normal ramp-up rate:** For transitions between energy output levels <u>over the normal course of operation</u>. The default value is 100% of maximum current output per second with a range of adjustment between 1% to 100%, with specific setting as mutually agreed by the Distributor Provider and the Producer.

ii) **Connect/Reconnect ramp-up rate:** Upon starting to inject power into the grid, following a period of inactivity or a disconnection, the inverter shall be able to control its rate of increase of power from 1 to 100% maximum current per second, with specific settings as mutually agreed upon by the Distributer Provider and the Producer.

Table 3: Normal and Soft Ramp Rate requirements (source SDG&E).

Note: the ramp rates are not specifically defined, and are likely to vary, based on local interconnection requirements, Ideal Power's factory defaults are set to the following:
- *Normal Ramp Rate: 4 kW/second*
- *Connect/Reconnect (also known as Soft) Ramp Rate: 1 kW/second.*
- *Both Ramp Rates are adjustable to the specified 1 to 100% maximum current per second as defined above.*

Region	Voltage at Point of Common Coupling (% Nominal Voltage)	Ride-Through Until	Operating Mode	Maximum Trip Time
High Voltage 2 (HV2)	V ≥120			0.16 sec.
High Voltage 1 (HV1)	110 < V < 120	12 sec.	Momentary Cessation	13 sec.
Near Nominal (NN)	88 ≤ V ≤ 110	Indefinite	Continuous Operation	Not Applicable
Low Voltage 1 (LV1)	70 ≤ V < 88	20 sec.	Mandatory Operation	21 sec.
Low Voltage 2 (LV2)	50 ≤ V < 70	10 sec.	Mandatory Operation	11 sec.
Low Voltage 3 (LV3)	V < 50	1 sec	Momentary Cessation	1.5 sec.

Table 2: Ideal Power Factory Default LVTR/HVRT Setpoints (source SDG&E).

System Frequency Default Settings (Hz)	Minimum Range of Adjustability (Hz)	Ride-Through Until	Ride-Through Operational Mode	MaximumTrip Time
f > 62	62 - 64	No Ride Through	Not Applicable	0.16 seconds
60.5 < f ≤ 62	60.1 - 62	299 seconds	Mandatory Operation	300 seconds
58.5 ≤ f ≤ 60.5	Not Applicable	Indefinite	Continuous Operation	Not Applicable
57.0 ≤ f < 58.5	57 - 59.9	299 seconds	Mandatory Operation	300 seconds
f < 57.0	53 - 57	No Ride Through	Not Applicable	0.16 seconds

Table 3: Ideal Power Factory Default LFTR/HFRT Setpoints (source SDG&E).

5.0 Advanced Features Programming

Section 5 details Converter Modbus registers and their default factory setpoints which support the State of California's Rule 21 SRD.

5.1 Volt-VAR Registers (0x0200 – 0x0207)
The following registers define the Volt-VAR grid support function curve.

5.1.1 volt_var_v1
Address: 0x0200 (512)
Range: 0 – 360
Default: 249 (249 Vac – 89.9% of nominal 277 Vac)

The volt_var_v1 register defines the V1 level for the grid support Volt-VAR curve.

5.1.2 volt_var_q1
Address: 0x0201 (513)
Range: -2150 – 2150
Default: 800 (+8 kVar at 89.9% of nominal 277 Vac)

The volt_var_q1 register defines the Q1 level for the grid support Volt-VAR curve.

5.1.3 volt_var_v2

Address: 0x0202 (514)
Range: 0 – 360
Default: 263 (263 Vac – 94.9% of nominal 277 Vac)

The volt_var_v2 register defines the V2 level for the grid support Volt-VAR curve.

5.1.4 volt_var_q2

Address: 0x0203 (515)
Range: -2150 – 2150
Default: 0 (0 kVar at 94.9% of nominal 277 Vac)

The volt_var_q2 register defines the Q2 level for the grid support Volt-VAR curve.

5.1.5 volt_var_v3

Address: 0x0204 (516)
Range: 0 – 360
Default: 301 (301 Vac – 108.7% of nominal 277 Vac)

The volt_var_v3 register defines the V3 level for the grid support Volt-VAR curve.

5.1.6 volt_var_q3

Address: 0x0205 (517)
Range: -2150 – 2150
Default: 0 (0kVAR at 108.7% of nominal 277V)

The volt_var_q3 register defines the Q3 level for the grid support Volt-VAR curve.

5.1.7 volt_var_v4

Address: 0x0206 (518)
Range: 0 – 360
Default: 318 (318 Vac – 114.8% of nominal 277 Vac)

The volt_var_v4 register defines the V4 level for the grid support Volt-VAR curve.

5.1.8 volt_var_q4

Address: 0x0207 (519)
Range: -2150 – 2150
Default: -800 (-8 kVar at 114.8% of nominal 277 Vac)

The volt_var_q4 register defines the Q4 level for the grid support Volt-VAR curve.

5.2 Freq-Watt Registers (0x0210 – 0x0217)
The following registers define the Freq-Watt grid support function parameter set.

5.2.1 freq_watt_lo_stop
Address: 0x0211 (529)
Range: 0 – 65000
Default: 58500 (58.5 Hz)

The freq_watt_lo_stop register defines the under-frequency point at which:
   a. AC1 import power is derated to 0 W
   b. AC1 export power is increased to 2 *x* pre-disturbance level (Export power can only be increased by Freq-Watt function if AC1 is set for constant power control and bit 9 is set in register grid_support_control).

5.2.2 freq_watt_lo_start
Address: 0x0212 (530)
Range: 0 – 65000
Default: 59750 (59.75 Hz)

The freq_watt_lo_start register defines the under-frequency point at which power derating or increase begins.

5.2.3 freq_watt_lo_safe
Address: 0x0213 (531)
Range: 0 – 65000
Default: 59850 (59.85 Hz)

The freq_watt_lo_safe register defines the under-frequency point at which the return-to-service timer is engaged. If Freq-Watt hysteresis is enabled via bit 8 in register grid_support_control, then when this timer expires, the PCS will return to its pre-disturbance power level. This register is unused if Freq-Watt hysteresis is disabled.

5.2.4 freq_watt_safetime
Address: 0x0214 (532)
Range: 1 – 180
Default: 60 (60 sec)

The freq_watt_safetime register defines the return-to-service timer for the Freq-Watt function if hysteresis is enabled. This register is set in units of 1 sec. This register is unused if Freq-Watt hysteresis is disabled.

5.2.5 freq_watt_hi_safe
Address: 0x0215 (533)
Range: 0 – 65000
Default: 60150 (60.15 Hz)

The freq_watt_hi_safe register defines the over-frequency point at which the return-to-service timer is engaged. If Freq-Watt hysteresis is enabled via bit 8 in register grid_support_control, then when this timer expires, the PCS will return to its pre-disturbance power level. This register is unused if Freq-Watt hysteresis is disabled.

5.2.6 freq_watt_hi_start
Address: 0x0216 (534)
Range: 0 – 65000
Default: 60250 (60.25 Hz)

The freq_watt_hi_start register defines the over-frequency point at which power derating or increase begins.

5.2.7 freq_watt_hi_stop
Address: 0x0217 (535)
Range: 0 – 65000
Default: 62000 (62.0 Hz)

The freq_watt_hi_stop register defines the over-frequency point at which:
   a. AC1 export power is derated to 0W
   b. AC1 import power is increased to 2 *x* pre-disturbance level (Import power can only be increased by Freq-Watt function if AC1 is set for constant power control and bit 9 is set in register grid_support_control).

5.3 Volt-Watt Registers (0x0218 – 0x021F)
The following registers define the Volt-Watt grid support function parameter set.

5.3.1 volt_watt_lo_stop
Address: 0x0218 (536)
Range: 0 – 360

Default: 249 (249 Vac – 89.9% of nominal 277 Vac)

The volt_watt_lo_stop register defines the under-voltage point at which:
   c. AC1 import power is derated to 0W
   d. AC1 export power is increased to 2 *x* pre-disturbance level (Export power can only be increased by Volt-Watt function if AC1 is set for constant power control and bit 11 is set in register grid_support_control).

5.3.2 volt_watt_lo_start
Address: 0x0219 (537)
Range: 0 – 360
Default: 263 (263 Vac – 94.9% of nominal 277 Vac)

The volt_watt_lo_start register defines the under-voltage point at which power derating or increase begins.

5.3.3 volt_watt_lo_safe
Address: 0x021A (538)
Range: 0 – 360
Default: 266 (266 Vac – 96% of nominal 277 Vac)

This register is reserved for future use, and is not utilized to support CA Rule 21.

5.3.4 volt_watt_safetime
Address: 0x021B (539)
Range: 1 – 180
Default: 60 (60 sec)

This register is reserved for future use, and is not utilized to support CA Rule 21.

5.3.5 volt_watt_hi_safe
Address: 0x021C (540)
Range: 0 – 360
Default: 294 (294 Vac – 106.1% of nominal 277 Vac)

This register is reserved for future use, and is not utilized to support CA Rule 21.

5.3.6 volt_watt_hi_start
Address: 0x021D (541)

Range: 0 – 360
Default: 301 (301 Vac – 108.7% of nominal 277 Vac)

The volt_watt_hi_start register defines the over-voltage point at which power derating or increase begins.

5.3.7 volt_watt_hi_stop
Address: 0x021E (542)
Range: 0 – 360
Default: 318 (318 Vac – 114.8% of nominal 277 Vac)

The volt_watt_hi_stop register defines the over-voltage point at which:
  c. AC1 export power is derated to 0W
  d. AC1 import power is increased to 2 *x* pre-disturbance level (Import power can only be increased by Volt-Watt function if AC1 is set for constant power control and bit 11 is set in register grid_support_control).

5.4 Low Voltage (LV) Disconnect and Ride-through Control Registers (0x0240 – 0x025F)
The following registers support the low voltage ride-through and disconnect functions of the PCS system.

5.4.1 uv_1_disco_level
Address: 0x0240 (576)
Range: 0 – 360
Default: 244 (244 Vac - 88% of nominal 277 Vac)

The uv_1_disco_level register defines the LV1 under-voltage region threshold. If the grid RMS voltage drops below this level for the duration set by register uv_1_disco_time, the PCS will fault, and cease power conversion. If set to 0, the LV1 region and its associated checks are disabled.

5.4.2 uv_1_disco_time
Address: 0x0242 (578)
Range: NA
Default: 2050 (20.5 sec)

The uv_1_disco_time register defines the LV1 under-voltage region ride-through time. If the grid RMS voltage drops below the LV1 threshold for the duration set by this register, the PCS will issue a fault, and cease power conversion.

5.4.3 uv_1_stop_level

Address: 0x0243 (579)
Range: 0 – 360
Default: 244 (244 Vac - 88% of nominal 277 Vac)

The uv_1_stop_level register defines the LV1 under-voltage region stop limit. If the grid RMS voltage is less than this register, the behavior programmed by register uv_1_ridethru_op will be set.

5.4.4 uv_1_stop_time

Address: 0x0245 (581)
Range: NA
Default: 1950 (19.5 sec)

The uv_1_stop_time register defines the LV1 under-voltage region time to stop. If the grid RMS voltage drops below the LV1 threshold set by register uv_1_stop_level for the duration set by this register, the PCS will stop exporting AC power, but NOT fault (cessation).

5.4.5 uv_1_ridethru_op

Address: 0x0246 (582)
Range: 0 – 1
Default: 0

The uv_1_ridethru_op register defines the behavior taken while the grid RMS voltage is within the LV1 under-voltage ride-through region.
uv_1_ridethru_op
  0 – Wait for duration set by register uv_1_stop_time before stopping power flows.
  1 – Immediately stop power flows.
In either case, the PCS system will stop AC power flows without faulting. The default behavior for LV1 ride-through is to wait for duration set by register uv_1_stop_time.

5.4.6 uv_2_disco_level

Address: 0x0247 (583)
Range: 0 – 360
Default: 194 (194 Vac - 70% of nominal 277 Vac)

The uv_2_disco_level register defines the LV2 under-voltage region threshold. If the grid RMS voltage drops below this level for the duration set by register uv_2_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion. If this register is set to 0, the LV2 region and its associated checks are disabled.

5.4.7 uv_2_disco_time

Address: 0x0249 (585)
Range: NA
Default: 1050 (10.5 sec)

The uv_2_disco_time register defines the LV2 under-voltage region ride-through time. If the grid RMS voltage drops below the LV2 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion.

5.4.8 uv_2_stop_level

Address: 0x024A (586)
Range: 0 – 360
Default: 194 (194 Vac - 70% of nominal 277 Vac)

The uv_2_stop_level register defines the LV2 under-voltage region stop limit. If the grid RMS voltage is less than this register, the behavior programmed by register uv_2_ridethru_op will be set.5.4.9 uv_2_stop_time
Address: 0x024C (588)
Range: NA
Default: 950 (9.5 sec)

The uv_2_stop_time register defines the LV2 under-voltage region time to stop. If the grid RMS voltage drops below the LV2 threshold set by register uv_2_stop_level for the duration set by this register, then the PCS will stop exporting AC power, but not fault.

5.4.10 uv_2_ridethru_op

Address: 0x024D (589)
Range: 0 – 1
Default: 0

The uv_2_ridethru_op register defines the behavior taken while the grid RMS voltage is within the LV2 under-voltage ride-through region.
uv_2_ridethru_op[0] –
      0 – Wait for duration set by register uv_2_stop_time before stopping power output.
      1 – Immediately stop power output.
In either case, the PCS system will stop AC current export without disconnecting from the AC1 port while in this region. The default behavior for LV2 ride-through is to wait for duration set by register uv_2_stop_time.

5.4.11 uv_3_disco_level
Address: 0x024E (590)
Range: 0 – 360
Default: 138.5 (138.5 Vac - 50% of nominal 277 Vac)

The uv_3_disco_level register defines the LV3 under-voltage region threshold. If the grid RMS voltage drops below this level for the duration set by register uv_3_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion. If this register is set to 0, the LV3 region and its associated checks are disabled.

5.4.12 uv_3_disco_time
Address: 0x0250 (592)
Range: NA
Default: 120 (1.2 sec)

The uv_3_disco_time register defines the LV3 under-voltage region ride-through time. If the grid RMS voltage drops below the LV3 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion.

5.4.13 uv_3_stop_level
Address: 0x0251 (593)
Range: 0 – 360
Default: 138.5 (138.5 Vac - 50% of nominal 277 Vac)

The uv_3_stop_level register defines the LV3 under-voltage region stop limit. If the grid RMS voltage is less than this register, the behavior programmed by register uv_3_ridethru_op will be set.

5.4.14 uv_3_stop_time
Address: 0x0253 (595)
Range: NA
Default: 90 (0.9 sec)

The uv_3_stop_time register defines the LV3 under-voltage region time to stop. If the grid RMS voltage drops below the LV3 threshold set by register uv_3_stop_level for the duration set by this register, then the PCS will stop exporting AC power and remain connected.

5.4.15 uv_3_ridethru_op
Address: 0x0254 (596)
Range: 0 – 1

Default: 1

The uv_3_ridethru_op register defines the behavior taken while the grid RMS voltage is within the LV3 under-voltage ride-through region.
uv_3_ridethru_op[0] –
       0 – Wait for duration set by register uv_3_stop_time before stopping power output.
       1 – Immediately stop power output.
In either case, the PCS system will stop AC current export without disconnecting from the AC1 port while in this region. The default behavior for LV3 ride-through is to immediately stop power output.

5.4.16 uv_4_disco_level
Address: 0x0255 (597)
Range: 0 – 360
Default: 0

This register is reserved for future use, and is not utilized to support CA Rule 21.

5.4.17 uv_4_disco_time
Address: 0x0257 (599)
Range: NA
Default: 0

This register is reserved for future use, and is not utilized to support CA Rule 21.

5.4.18 uv_4_stop_level
Address: 0x0258 (600)
Range: 0 – 360
Default: 0 (Disabled)

This register is reserved for future use, and is not utilized to support CA Rule 21.

5.4.19 uv_4_stop_time
Address: 0x025A (602)
Range: NA
Default: 0

This register is reserved for future use, and is not utilized to support CA Rule 21.

5.4.20 uv_4_ridethru_op
Address: 0x025B (603)
Range: 0 – 1
Default: 0

This register is reserved for future use, and is not utilized to support CA Rule 21.

5.5 High Voltage (HV) Disconnect and Ride-through Control Registers (0x0260 – 0x027F)
The following registers support the high voltage ride-through and disconnect functions of the PCS.

5.5.1 ov_1_disco_level
Address: 0x0260 (608)
Range: 0 – 360
Default: 305 (305 Vac - 110% of nominal 277 Vac)

The ov_1_disco_level register defines the HV1 over-voltage region threshold. If the grid RMS voltage rises above this level for the duration set by register ov_1_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion, and disconnect from the AC1 port. If this register is set to 0, the HV1 region and its associated checks are disabled.

5.5.2 ov_1_disco_time
Address: 0x0262 (610)
Range: NA
Default: 1250 (12.5 sec)

The ov_1_disco_time register defines the HV1 over-voltage region ride-through time. If the grid RMS voltage drops below the HV1 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion.

5.5.3 ov_1_stop_level
Address: 0x0263 (611)
Range: 0 – 360
Default: 305 (305 Vac - 110% of nominal 277 Vac)

The ov_1_stop_level register defines the HV1 over-voltage region stop limit. If the grid RMS voltage is above this register, the behavior programmed by register ov_1_ridethru_op will be set.

5.5.4 ov_1_stop_time

Address: 0x0265 (613)
Range: NA
Default: 1150 (11.5 sec)

The ov_1_stop_time register defines the HV1 over-voltage region time to stop. If the grid RMS voltage rises above the HV1 threshold set by register ov_1_stop_level for the duration set by this register, then the PCS will stop exporting AC power and remain connected.

5.5.5 ov_1_ridethru_op

Address: 0x0266 (614)
Range: 0 – 1
Default: 1

The ov_1_ridethru_op register defines the behavior taken while the grid RMS voltage is within the HV1 over-voltage ride-through region.
ov_1_ridethru_op[0] –
       0 – Wait for duration set by register ov_1_stop_time before stopping power output.
       1 – Immediately stop power output.
In either case, the PCS system will stop AC current exporting while in this region. The default behavior for HV1 ride-through is to wait for duration set by register ov_1_stop_time.

5.5.6 ov_2_disco_level

Address: 0x0267 (615)
Access: RW

Range: 0 – 360
Default: 332 (332 Vac - 120% of nominal 277 Vac)

The ov_2_disco_level register defines the HV2 over-voltage region threshold. If the grid RMS voltage rises above this level for the duration set by register ov_2_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion. If this register is set to 0, the HV2 region and its associated checks are disabled.

5.5.7 ov_2_disco_time

Address: 0x0269 (617)
Range: NA
Default: 13 (0.13 sec)

The ov_2_disco_time register defines the HV2 over-voltage region ride-through time. If the grid RMS voltage rises above the HV2 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion.

5.5.8 ov_2_stop_level
Address: 0x026A (618)
Range: 0 – 360
Default: 332 (332 Vac - 120% of nominal 277 Vac)

The ov_2_stop_level register defines the HV2 over-voltage region stop limit. If the grid RMS voltage is above this register, the behavior programmed by register ov_2_ridethru_op will be set.

5.5.9 ov_2_stop_time
Address: 0x026C (620)
Range: NA
Default: 13 (0.13 sec)

The ov_2_stop_time register defines the HV2 over-voltage region time to stop. If the grid RMS voltage rises above the HV2 threshold set by register ov_2_stop_level for the duration set by this register, then the PCS will stop exporting AC power and remain connected.

5.5.10 ov_2_ridethru_op
Address: 0x026D (621)
Range: 0 – 1
Default: 0

The ov_2_ridethru_op register defines the behavior taken while the grid RMS voltage is within the HV2 over-voltage ride-through region.
ov_2_ridethru_op[0] –
    0 – Wait for duration set by register ov_2_stop_time before stopping power output.
    1 – Immediately stop power output.
In either case, the PCS system will stop AC current export without disconnecting from the AC1 port while in this region. The default behavior for HV2 ride-through is to wait for duration set by register ov_2_stop_time.

5.5.11 ov_3_disco_level
Address: 0x026E (622)
Range: 0 – 360
Default: 0

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The ov_3_disco_level register defines the HV3 over-voltage region threshold. If the grid RMS voltage rises above this level for the duration set by register ov_3_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion. If this register is set to 0, the HV3 region and its associated checks are disabled.

5.5.12 ov_3_disco_time
Address: 0x0270 (624)
Range: NA
Default: 0

The ov_3_disco_time register defines the HV3 over-voltage region ride-through time. If the grid RMS voltage rises above the HV3 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion. 5.5.13 ov_3_stop_level
Address: 0x0271 (625)
Range: 0 – 360
Default: 0 (Disabled)

The ov_3_stop_level register defines the HV3 over-voltage region stop limit. If the grid RMS voltage is above this register, the behavior programmed by register ov_3_ridethru_op will be set.

5.5.14 ov_3_stop_time
Address: 0x0273 (627)
Range: NA
Default: 0

The ov_3_stop_time register defines the HV3 over-voltage region time to stop. If the grid RMS voltage rises above the HV3 threshold set by register ov_3_stop_level for the duration set by this register, then the PCS will stop exporting AC power and remain connected. This register is specified in units of 10 msec.

5.5.15 ov_3_ridethru_op
Address: 0x0274 (628)
Range: 0 – 1
Default: 0

The ov_3_ridethru_op register defines the behavior taken while the grid RMS voltage is within the HV3 over-voltage ride-through region.

ov_3_ridethru_op[0] –
　　　　0 – Wait for duration set by register ov_3_stop_time before stopping power output.
　　　　1 – Immediately stop power output.
In either case, the PCS system will stop AC exporting but not fault.. The default behavior for
HV3 ride-through is to immediately stop power output.

5.5.16 ov_4_disco_level
Address: 0x0275 (629)
Range: 0 – 360
Default: 0

The ov_4_disco_level register defines the HV4 over-voltage region threshold. If the grid RMS
voltage rises above this level for the duration set by register ov_4_disco_time, then the PCS will
issue an ABORT-0 fault, and stop power conversion. If this register is set to 0, the HV4 region
and its associated checks are disabled.

5.5.17 ov_4_disco_time
Address: 0x0277 (631)
Range: NA
Default: 0

The ov_4_disco_time register defines the HV4 over-voltage region ride-through time. If the grid
RMS voltage rises above the HV4 threshold for the duration set by this register, then the PCS
will issue an ABORT-0 fault, and stop power conversion. This register is specified in units of 10
msec.

5.5.18 ov_4_stop_level
Address: 0x0278 (632)
Range: 0 – 360
Default: 0 (Disabled)

The ov_4_stop_level register defines the HV4 over-voltage region stop limit. If the grid RMS
voltage is above this register, the behavior programmed by register ov_4_ridethru_op will be
set.

5.5.19 ov_4_stop_time
Address: 0x027A (634)
Range: NA
Default: 0

The ov_4_stop_time register defines the HV4 over-voltage region time to stop. If the grid RMS voltage rises above the HV4 threshold set by register ov_4_stop_level for the duration set by this register, then the PCS will stop exporting AC power and remain connected. This register is specified in units of 10 msec.

5.5.20 ov_4_ridethru_op
Address: 0x027B (635)
Range: 0 – 1
Default: 0

The ov_4_ridethru_op register defines the behavior taken while the grid RMS voltage is within the HV4 over-voltage ride-through region.
ov_4_ridethru_op[0] –
      0 – Wait for duration set by register ov_4_stop_time before stopping power output.
      1 – Immediately stop power output.
In either case, the PCS system will stop AC exporting, but not fault. This region is not implemented by default.

5.6 Low Frequency (LF) Disconnect and Ride-through Control Registers (0x0280 – 0x029F)
The following registers support the low frequency ride-through and disconnect functions of the PCS.

5.6.1 uf_1_disco_level
Address: 0x0280 (640)
Range: 0 – 65000
Default: 58500 (58.5 Hz)

The uf_1_disco_level register defines the LF1 under-frequency region threshold. If the grid frequency drops below this level for the duration set by register uf_1_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion. If this register is set to 0, the LF1 region and its associated checks are disabled.

5.6.2 uf_1_disco_time
Address: 0x0282 (642)
Range: NA
Default: 29950 (299.5 sec)

The uf_1_disco_time register defines the LF1 under-frequency region ride-through time. If the grid frequency drops below the LF1 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion.

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5.6.3 uf_1_stop_level

Address: 0x0283 (643)
Range: 0 – 65000
Default: 58500 (58.5Hz)

The uf_1_stop_level register defines the LF1 under-frequency region stop limit. If the grid frequency is less than this register, the behavior programmed by register uf_1_ridethru_op will be set.

5.6.4 uf_1_stop_time

Address: 0x0285 (645)
Range: NA
Default: 29870 (298.70 sec)

The uf_1_stop_time register defines the LF1 under-frequency region time to stop. If the grid frequency drops below the LF1 threshold set by register uf_1_stop_level for the duration set by this register, then the PCS will stop exporting AC power and remain connected.

5.6.5 uf_1_ridethru_op

Address: 0x0286 (646)
Range: 0 – 1
Default: 0

The uf_1_ridethru_op register defines the behavior taken while the grid frequency is within the LF1 under-frequency ride-through region.
uf_1_ridethru_op[0] –
      0 – Wait for duration set by register uf_1_stop_time before stopping power output.
      1 – Immediately stop power output.
In either case, the PCS system will stop AC exporting without faulting while in this region. The default behavior for LF1 ride-through is to wait for duration set by register uf_1_stop_time.

5.6.6 uf_2_disco_level

Address: 0x0287 (647)
Range: 0 – 65000
Default: 57000 (57.0 Hz)

The uf_2_disco_level register defines the LF2 under-frequency region threshold. If the grid frequency drops below this level for the duration set by register uf_2_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion. If this register is set to 0, the LF2 region and its associated checks are disabled.

5.6.7 uf_2_disco_time
Address: 0x0289 (649)
Range: NA
Default: 13 (0.13 sec)

The uf_2_disco_time register defines the LF2 under-frequency region ride-through time. If the grid frequency drops below the LF2 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion.

5.6.8 uf_2_stop_level
Address: 0x028A (650)
Range: 0 – 65000
Default: 57000 (57.0 Hz)

The uf_2_stop_level register defines the LF2 under-frequency region stop limit. If the grid frequency is less than this register, the behavior programmed by register uf_2_ridethru_op will be set.

5.6.9 uf_2_stop_time
Address: 0x028C (652)
Range: NA
Default: 13 (0.13 sec)

The uf_2_stop_time register defines the LF2 under-frequency region time to stop. If the grid frequency drops below the LF2 threshold set by register uf_2_stop_level for the duration set by this register, then the PCS will stop exporting AC power, but not fault.

5.6.10 uf_2_ridethru_op
Address: 0x028D (653)
Range: 0 – 1
Default: 0

The uf_2_ridethru_op register defines the behavior taken while the grid frequency is within the LF2 under-frequency ride-through region.
uf_2_ridethru_op[0] –
      0 – Wait for duration set by register uf_2_stop_time before stopping power output.
      1 – Immediately stop power output.
In either case, the PCS system will stop AC current export without disconnecting from the AC1 port while in this region. The default behavior for LF2 ride-through is to wait for duration set by register uf_2_stop_time.

5.6.11 uf_3_disco_level

Address: 0x028E (654)
Range: 0 – 65000
Default: 0 (Disabled)

The uf_3_disco_level register defines the LF3 under-frequency region threshold. If the grid frequency drops below this level for the duration set by register uf_3_disco_time, then the PCS will issue an ABORT-0 fault, stop power conversion, and disconnect from the AC1 port. If this register is set to 0, the LF3 region and its associated checks are disabled.

5.6.12 uf_3_disco_time

Address: 0x0290 (656)
Range: NA
Default: 0

The uf_3_disco_time register defines the LF3 under-frequency region ride-through time. If the grid frequency drops below the LF3 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion. This register is specified in units of 10 msec.

5.6.13 uf_3_stop_level

Address: 0x0291 (657)
Range: 0 – 65000
Default: 0 (Disabled)

The uf_3_stop_level register defines the LF3 under-frequency region stop limit. If the grid frequency is less than this register, the behavior programmed by register uf_3_ridethru_op will be set. This register is set in units of 0.001Hz.

5.6.14 uf_3_stop_time

Address: 0x0293 (659)
Range: NA
Default: 0

The uf_3_stop_time register defines the LF3 under-frequency region time to stop. If the grid frequency drops below the LF3 threshold set by register uf_3_stop_level for the duration set by this register, then the PCS will stop exporting AC power and remain connected. This register is specified in units of 10 msec.

5.6.15 uf_3_ridethru_op

Address: 0x0294 (660)

Range: 0 – 1

Default: 0

The uf_3_ridethru_op register defines the behavior taken while the grid frequency is within the LF3 under-frequency ride-through region.

uf_3_ridethru_op[0] –

        0 – Wait for duration set by register uf_3_stop_time before stopping power output.

        1 – Immediately stop power output.

In either case, the PCS system will stop AC current export without faulting. The default behavior for LF3 ride-through is to immediately stop power output.

5.6.16 uf_4_disco_level

Address: 0x0295 (661)

Access: RW

Default: 0 (Disabled)

The uf_4_disco_level register defines the LF4 under-frequency region threshold. If the grid frequency drops below this level for the duration set by register uf_4_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion. This register is specified in units of 0.001Hz. If this register is set to 0, the LF4 region and its associated checks are disabled.

5.6.17 uf_4_disco_time

Address: 0x0297 (663)

Range: NA

Default: 0

The uf_4_disco_time register defines the LF4 under-frequency region ride-through time. If the grid frequency drops below the LF4 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion. This register is specified in units of 10 msec.

5.6.18 uf_4_stop_level

Address: 0x0298 (664)

Range: 0 – 65000

Default: 0 (Disabled)

The uf_4_stop_level register defines the LF4 under-frequency region stop limit. If the grid frequency is less than this register, the behavior programmed by register uf_4_ridethru_op will be set. This register is set in units of 0.001Hz.

5.6.19 uf_4_stop_time
Address: 0x029A (666)
Range: NA
Default: 0

The uf_4_stop_time register defines the LF4 under-frequency region time to stop. If the grid frequency drops below the LF4 threshold set by register uf_4_stop_level for the duration set by this register, then the PCS will stop exporting and remain connected. This register is specified in units of 10 msec.

5.6.20 uf_4_ridethru_op
Address: 0x029B (667)
Range: 0 – 1
Default: 0

The uf_4_ridethru_op register defines the behavior taken while the grid frequency is within the LF4 under-frequency ride-through region.
uf_4_ridethru_op[0] –
      0 – Wait for duration set by register uf_4_stop_time before stopping power output.
      1 – Immediately stop power output.
In either case, the PCS system will stop AC current export without disconnecting from the AC1 port while in this region. This region is not implemented by default.

5.7 High Frequency (HF) Disconnect and Ride-through Control Registers (0x02A0 – 0x02BF)
The following registers support the high frequency ride-through and disconnect functions of the PCS system.

5.7.1 of_1_disco_level
Address: 0x02A0 (672)
Range: 0 – 65000
Default: 60500 (60.5 Hz)

The of_1_disco_level register defines the HF1 over-frequency region threshold. If the grid frequency rises above this level for the duration set by register of_1_disco_time, then the PCS will issue an ABORT-0 fault, stop power conversion, and disconnect from the AC1 port. This

register is specified in units of 0.001Hz. If this register is set to 0, the HF1 region and its associated checks are disabled.

5.7.2 of_1_disco_time
Address: 0x02A2 (674)
Range: NA
Default: 29950 (299.5 sec)

The of_1_disco_time register defines the HF1 over-frequency region ride-through time. If the grid frequency rises above the HF1 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion.

5.7.3 of_1_stop_level
Address: 0x02A3 (675)
Range: 0 – 65000
Default: 60500 (60.5 Hz)

The of_1_stop_level register defines the HF1 over-frequency region stop limit. If the grid frequency is less than this register, the behavior programmed by register of_1_ridethru_op will be set.

5.7.4 of_1_stop_time
Address: 0x02A5 (677)
Range: NA
Default: 29870 (298.70 sec)

The of_1_stop_time register defines the HF1 over-frequency region time to stop. If the grid frequency rises above the HF1 threshold set by register of_1_stop_level for the duration set by this register, then the PCS will stop exporting AC power and remain connected (no fault).

5.7.5 of_1_ridethru_op
Address: 0x02A6 (678)
Range: 0 – 1
Default: 0

The of_1_ridethru_op register defines the behavior taken while the grid frequency is within the HF1 over-frequency ride-through region.
of_1_ridethru_op[0] –
    0 – Wait for duration set by register of_1_stop_time before stopping power output.
    1 – Immediately stop power output.

In either case, the PCS system will stop AC exporting, without faultingwhile in this region. The default behavior for HF1 ride-through is to wait for duration set by register of_1_stop_time.

5.7.6 of_2_disco_level
Address: 0x02A7 (679)
Range: 0 – 65000
Default: 62000 (62.0 Hz)

The of_2_disco_level register defines the HF2 over-frequency region threshold. If the grid frequency rises above this level for the duration set by register of_2_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion. If this register is set to 0, the HF2 region and its associated checks are disabled.

5.7.7 of_2_disco_time
Address: 0x02A9 (681)
Range: NA
Default: 13 (0.13 sec)

The of_2_disco_time register defines the HF2 over-frequency region ride-through time. If the grid frequency rises above the HF2 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion.

5.7.8 of_2_stop_level
Address: 0x02AA (682)
Range: 0 – 65000
Default: 62000 (62.0 Hz)

The of_2_stop_level register defines the HF2 over-frequency region stop limit. If the grid frequency is less than this register, the behavior programmed by register of_2_ridethru_op will be set.

5.7.9 of_2_stop_time
Address: 0x02AC (684)
Access: RW
Default: 13 (0.13 sec)

The of_2_stop_time register defines the HF2 over-frequency region time to stop. If the grid frequency rises above the HF2 threshold set by register of_2_stop_level for the duration set by this register, then the PCS will stop exporting AC power, but not fault.

5.7.10 of_2_ridethru_op
Address: 0x02AD (685)
Range: 0 – 1
Default: 0

The of_2_ridethru_op register defines the behavior taken while the grid frequency is within the HF2 over-frequency ride-through region.
of_2_ridethru_op[0] –
        0 – Wait for duration set by register of_2_stop_time before stopping power output.
        1 – Immediately stop power output.
In either case, the PCS system will stop AC current export without faulting while in this region. The default behavior for HF2 ride-through is to wait for duration set by register of_2_stop_time.

5.7.11 of_3_disco_level
Address: 0x02AE (686)
Range: 0 – 65000
Default: 0 (Disabled)

The of_3_disco_level register defines the HF3 over-frequency region threshold. If the grid frequency rises above this level for the duration set by register of_3_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion.

5.7.12 of_3_disco_time
Address: 0x02B0 (688)
Range: NA
Default: 0

The of_3_disco_time register defines the HF3 over-frequency region ride-through time. If the grid frequency rises above the HF3 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion. This register is specified in units of 10 msec.

5.7.13 of_3_stop_level
Address: 0x02B1 (689)
Range: 0 – 65000
Default: 0 (Disabled)

The of_3_stop_level register defines the HF3 over-frequency region stop limit. If the grid frequency is less than this register, the behavior programmed by register of_3_ridethru_op will be set. This register is set in units of 0.001Hz.

5.7.14 of_3_stop_time
Address: 0x02B3 (691)
Range: NA
Default: 0

The of_3_stop_time register defines the HF3 over-frequency region time to stop. If the grid frequency rises above the HF3 threshold set by register of_3_stop_level for the duration set by this register, then the PCS will stop exporting, but not fault. This register is specified in units of 10 msec.

5.7.15 of_3_ridethru_op
Address: 0x02B4 (692)
Range: 0 – 1
Default: 0

The of_3_ridethru_op register defines the behavior taken while the grid frequency is within the HF3 over-frequency ride-through region.
of_3_ridethru_op[0] –
   0 – Wait for duration set by register of_3_stop_time before stopping power output.
   1 – Immediately stop power output.
In either case, the PCS system will stop AC exporting, but not fault. while in this region. The default behavior for HF3 ride-through is to immediately stop power output.

5.7.16 of_4_disco_level
Address: 0x02B5 (693)
Range: 0 – 65000
Default: 0 (Disabled)

The of_4_disco_level register defines the HF4 over-frequency region threshold. If the grid frequency rises above this level for the duration set by register of_4_disco_time, then the PCS will issue an ABORT-0 fault, and stop power conversion. This register is specified in units of 0.001Hz. If this register is set to 0, the HF4 region and its associated checks are disabled.

5.7.17 of_4_disco_time
Address: 0x02B7 (695)
Range: NA

Default: 0

The of_4_disco_time register defines the HF4 over-frequency region ride-through time. If the grid frequency rises above the HF4 threshold for the duration set by this register, then the PCS will issue an ABORT-0 fault, and stop power conversion. This register is specified in units of 10 msec.

5.7.18 of_4_stop_level
Address: 0x02B8 (696)
Range: 0 – 65000
Default: 0 (Disabled)

The of_4_stop_level register defines the HF4 over-frequency region stop limit. If the grid frequency is less than this register, the behavior programmed by register of_4_ridethru_op will be set. This register is set in units of 0.001Hz.

5.7.19 of_4_stop_time
Address: 0x02BA (698)
Range: NA
Default: 0

The of_4_stop_time register defines the HF4 over-frequency region time to stop. If the grid frequency rises above the HF4 threshold set by register of_4_stop_level for the duration set by this register, then the PCS will stop exporting AC power and remain connected. This register is specified in units of 10 msec.

5.7.20 of_4_ridethru_op
Address: 0x02BB (699)
Range: 0 – 1
Default: 0

The of_4_ridethru_op register defines the behavior taken while the grid frequency is within the HF4 over-frequency ride-through region.
of_4_ridethru_op[0] –
      0 – Wait for duration set by register of_4_stop_time before stopping power output.
      1 – Immediately stop power output.
In either case, the PCS system will stop AC current export without disconnecting from the AC1 port while in this region. This region is not implemented by default.

5.8 p1_norm_power_ramp_rate

Address: 0x0042 (66)
Access: RW
Default: 400 (4 kW/sec)

The p1_norm_power_ramp_rate register defines the normal-operations power ramp rate used in constant active power control. This ramp rate is used only for normal power transitions after power conversion has started (going from one setpoint to another).

5.9 p1_power_factor_setpt

Address: 0x0046 (70)
Range: 70 – 130
Default: 100 (unity)

The p1_power_factor_setpt defines the setpoint when AC1 is set to control reactive power via constant power factor. This register is ignored if the AC1 port is set for constant reactive power control via register grid_support_control. The register is set in units of 0.01. The value entered in this register determines the effective signed power factor to control by the following equation:

$$pf(x) = \begin{cases} x - 200, & 130 > x > 100 \\ x, & 70 < x < 100 \end{cases}$$

For example, if p1_power_factor_setpt is set to 125, the PCS will set the observed power factor to -0.75. If the p1_power_factor_setpt register is set to 80, the PCS will set the observed power factor +0.80. *All IPWR PCS' use the IEEE power factor sign convention (positive in quadrants 2, 4; negative in quadrants 1, 3).*

5.10 p1_real_pwr_ramped

Address: 0x0064 (100)
Range: NA
Default: NA

The p1_real_pwr_ramped reads back the ramping control point for real power when the PCS is performing power conversion and the AC1 port is set for grid-following constant power control. The register is read back in units of 10W.

6.0 Enabling Advanced Inverter Features

The grid support control register provides control for the autonomous grid support functions in compliance with the UL1741-SA standard for grid support utility interactive inverters.

This is a hex read/write register at address 0x011E (286). The register bit structure is defined below, starting with the LSB:

- **[b0]** – Enable 'momentary cessation' feature. This forces the PCS to drop export AC current below 20% in the event of a voltage or frequency ride-thru events.
- **[b1]** – Enable PCS soft-ramping at startup and on reconnect after system faults.
- **[b2]** – Enable PCS power factor control, with setpoint determined by register p1_power_factor_setpt. If power factor control is enabled, the constant reactive component power control is disabled and the Volt-VAR function is disabled.
- **[b3]** – Enable PCS Volt-VAR grid support function. The Volt-VAR curve is specified by the register array starting at address 512 with points consisting of <volt, var> setpoints. If the Volt-VAR function is enabled, the constant power factor control is disabled.
- **[b4]** – Enable PCS Freq-WATT grid support function. The Freq-WATT parameter set is specified by the register array starting at address 529. If the Freq-WATT function is enabled, the Volt-WATT function is disabled.
- **[b5]** – Enable PCS Volt-WATT grid support function. The Volt-WATT parameter set is specified by the register array starting at address 536. If the Volt-WATT function is enabled, the Freq-WATT function is disabled.
- **[b6]** – Reserved
- **[b7]** – Reserved
- **[b8]** – Enable Freq-WATT hysteresis.
- **[b9]** – Enable Freq-WATT increase in power export due to frequency decrease *or* increase in power import due to frequency increase. This requires that the the PCS programmed for GPWR control method.
- **[b10]** – Enable Volt-WATT hysteresis.
- **[b11]** – Enable Volt-WATT increase in power export due to voltage decrease *or* increase in power import due to voltage increase. This ability requires that the PCS be programmed to the GPWR Control Method.

Notes:

1. The Freq-WATT and Volt-WATT functions cannot be enabled at the same time. The PCS system will give precedence to the Volt-WATT function if the user attempts to enable both simultaneously.

2. The specific power factor control and Volt-VAR functions cannot be enabled at the same time. The PCS system will give precedence to the Volt-VAR function if the user attempts to enable both simultaneously.

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Enable Volt-Watt /Disable Freq-Watt	Enable Freq-Watt /Disable Volt-Watt	Enable Volt-VAR /Disable SPF	Enable SPF control /Disable Volt-VAR	Enable soft-ramping	Enable momentary cessation
Bit	15	14	13	12	11	10	9	8
Description	Reserved				Enable Volt-Watt increase	Enable Volt-Watt hysteresis	Enable Freq-Watt increase	Enable Freq-Watt hysteresis

- END OF DOCUMENT -